REMARKS

Claims 1-4, 6-13, 15-21, 24 and 25 were examined and rejected. Applicants amend claims 1, 7-8, 11, 17 and 20. Applicants submit that no new matter is added therein, as the amendments to claims 1 and 20 are at least supported by Figures 3-5 and paragraphs 18, 27 and 42-43 of the application; the amendments to claim 7 are at least supported by paragraphs 19 and 21 of the application; and the amendments to claims 8, 11 and 17 are at least supported by Figures 3-5 and paragraphs 18, 25, 33-34, and 42-43 of the application, as originally filed. Applicants respectfully request reconsideration of amended claims 1-4, 6-13, 15-21 and 24-25 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. § 102

The Patent Office rejects claims 1-2 and 6-7 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,119,192 to Kao et al. (Kao). It is axiomatic that to be anticipated every limitation of the claim must be disclosed in a single reference.

Applicants respectfully disagree with the rejection above and submit that claim 1 is patentable over the cited references for at least the reason that the cited references do not disclose a non-volatile test memory storing information to load a plurality of configuration registers of a test device during a memory design validation test for a plurality of products to be manufactured, wherein the non-volatile memory has a maximum memory size less than a memory size sufficient to fill all the configuration registers, as required by amended claim 1. According to claim 1, for example, the maximum size of the test memory is not large enough to store all of the address information and data corresponding to the address information for all of the configuration registers of the test device during a memory design validation test for a plurality of products to be manufactured. Hence, less than all of the plurality of configuration registers of the device can be loaded using the data in the memory during a memory design validation test for a plurality of products to be manufactured.

Kao discloses an interface and memory for providing second initialization parameters from a supplemental parameter memory separate and distinct from the system BIOS memory (see column 2 lines 63-67) for personal computer systems which include both a PCI bus and an ISA bus (see column 1 lines 10-11) because the PCI bus is supported by a large number of personal computer system vendors as the standard of

choice (see column 1 lines 35-40). For instance, Kao, column 2 lines 42-26, describes a conventional initialization of a mass manufactured computer system.

However, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in the references of a non-volatile test memory storing information to load a plurality of configuration registers of a test device during a memory design validation test for a plurality of products to be manufactured, as required by claim 1.

Hence, for at least this reason, Applicants respectfully request the Patent Office withdraw the rejection above for claim 1.

II. Claims Rejected Under 35 U.S.C. § 103

The Patent Office rejects claims 3-4 and 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of U.S. Patent Application Serial No. 2004/0143715 to Bonaccio et al. (Bonaccio). To render a claim obvious, every limitation of that claim must be taught or suggested by at least one properly combined reference.

Claim 3 and 4 are submitted as not being anticipated or obvious in view of Kao for at least the same reasons given above in support of their base claim, claim 1. In addition, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in Bonaccio of a non-volatile test memory storing information to load a plurality of configuration registers of a test device during a memory design validation test for a plurality of products to be manufactured, as required by claim 1.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above for claims 3-4.

Applicants disagree with the rejection above for claim 8 for at least the reason that the references do not teach repeating the resetting and loading of a test device from a non-volatile test memory at least three times to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile memory during a memory design validation stage, as required by amended claim 8.

Kao discloses an interface and memory for providing second initialization parameters from a supplemental parameter memory separate and distinct from the system BIOS memory (see column 2 lines 63-67). Specifically, Kao only teaches and

only enables loading second initialization parameters from an I2C bus, and loading first initialization parameters from BIOS (see column 2 line 55 through column 3 line 60).

In addition, Bonaccio fails to cure the shortcomings of Kao. Specifically, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion of repeating during a memory design validation stage in Bonaccio.

Consequently, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in the references of repeating the resetting and loading of a test device from a non-volatile test memory at least three times to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile memory during a memory design validation stage, as required by amended claim 8.

Hence, for at least this reason, Applicants respectfully request the Patent Office withdraw the rejection above for claim 8.

The Patent Office rejects claims 11-13, 15-19, 24 and 25 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio and U.S. Patent No. 6,480,946 to Tomashima et al. (Tomashima).

Applicants respectfully disagree with the rejection above for claim 11 for at least the reason that the cited references do not teach or suggest loading during a memory design validation stage, identifying a subset of the plurality of test data that correspond to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration prior to loading, and manufacturing a plurality of products based on the test information and the subset, as required by amended claim 11. An argument analogous to the one above for claim 4 regarding Kao and Bonaccio not teaching a memory design validation test applies here to show that those references do not teach manufacturing a plurality of products based on the test information and the subset, as required by claim 11.

In addition, Tomashima fails to cure the shortcomings of the other references. Tomashima teaches reducing skew between read and write signals of a memory system including a plurality of discrete memory devices connected in parallel to a bus to transmit/receive signals to and from a commonly provided controller (see column 1 lines 7-15; column 6 lines 44-53). Also, Tomashima teaches a conventional memory controller performing this reduction by sending a command signal to Vernier circuit

300a during initialization of the memory devices (see column 6 lines 60-65; column 7 lines 30-33) during normal operational mode (see column 37 lines 33-39; column 8 lines 57-62; column 36 line 26 through column 37 line30; and column 38 lines 1-4). However, the initialization stages and operation of conventional memory systems of Tomashima do not teach loading during a memory design validation stage, identifying a subset of the plurality of test data that correspond to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration prior to loading, and manufacturing a plurality of products based on the test information and the subset, as required by claim 11.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above of claim 11.

In addition to the reasons above, Applicants submit that the motivation for combining Tomashima with Bonaccio or Kao is improper. Specifically, Bonaccio and Kao teach programming configuration registers using configuration sets stored in BIOS. On the other hand Tomashima teaches adjusting reference voltage Vref of a Vernier circuit to reduce skew between read and write signals to and from discrete memory devices of a memory system (see Figures 43 and 46; and column 35 line 28 through column 37 line 55). Specifically, Vref is updated using tap circuit 300a which includes a shift register circuit 315, gates, latches and switches (see column 38) which may be initialized by a command applied from the memory controller (see column 37 lines 1-10). Thus, there is no motivation or suggestion in Tomashima for resetting configuration registers and loading configuration registers using information stored in a nonvolatile memory. Consequently, the motivation for such a combination can be gleaned only from Applicants' specification. Hence, the combination is improper. Therefore, for at least this additional reason, Applicants respectfully request the Patent Office withdraw the rejections herein based on these references.

The Patent Office rejects claims 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio and U.S. Patent No. 5,737,524 to Cohen et al. (Cohen).

Applicants respectfully disagree with the rejection above for at least the reason that the cited references do not teach or suggest a plurality of test configuration

registers of an Ethernet controller device in a test laboratory, a non-volatile test memory in the test laboratory and configured to store information to load at least two of the plurality of configuration registers, and a block of test control logic in the test laboratory and coupled to the non-volatile memory to write the plurality of data to the plurality of configuration registers during a memory design validation test, as required by independent claim 20.

An argument analogous to the one above for claim 4 regarding Kao and Bonaccio not teaching a memory design validation test applies here to show that those references do not teach test configuration registers, a non-volatile test memory, and a block of test control logic in the test laboratory to write the plurality of data to the plurality of configuration registers during a memory design validation test, as required by claim 20.

Also, Cohen teaches loading configuration registers with information which is stored in a non-volatile storage (see column 2 lines 59-64). However, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in Cohen of the above noted configuration registers, a non-volatile test memory, and a block of test control logic in the test laboratory to write the plurality of data to the plurality of configuration registers during a memory design validation test limitations of claim 20.

Thus, none of Kao, Bonaccio, Cohen or their combination teaches or suggests the above noted limitation of claim 20.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above.

Any dependent claims not mentioned herein are submitted as not being anticipated or obvious for at least the reasons given above in support of their base claims and for the additional further limitations of those dependent claims. Hence, Applicants respectfully request the Patent Office withdraw the rejection above of all the claims.

CONCLUSION

In view of the foregoing, it is believed that all claims now are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Angelo J. Gaz, Reg. No. 45,907

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(310) 207-3800

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Angelo J. Gaz — Date: 12/26/07